

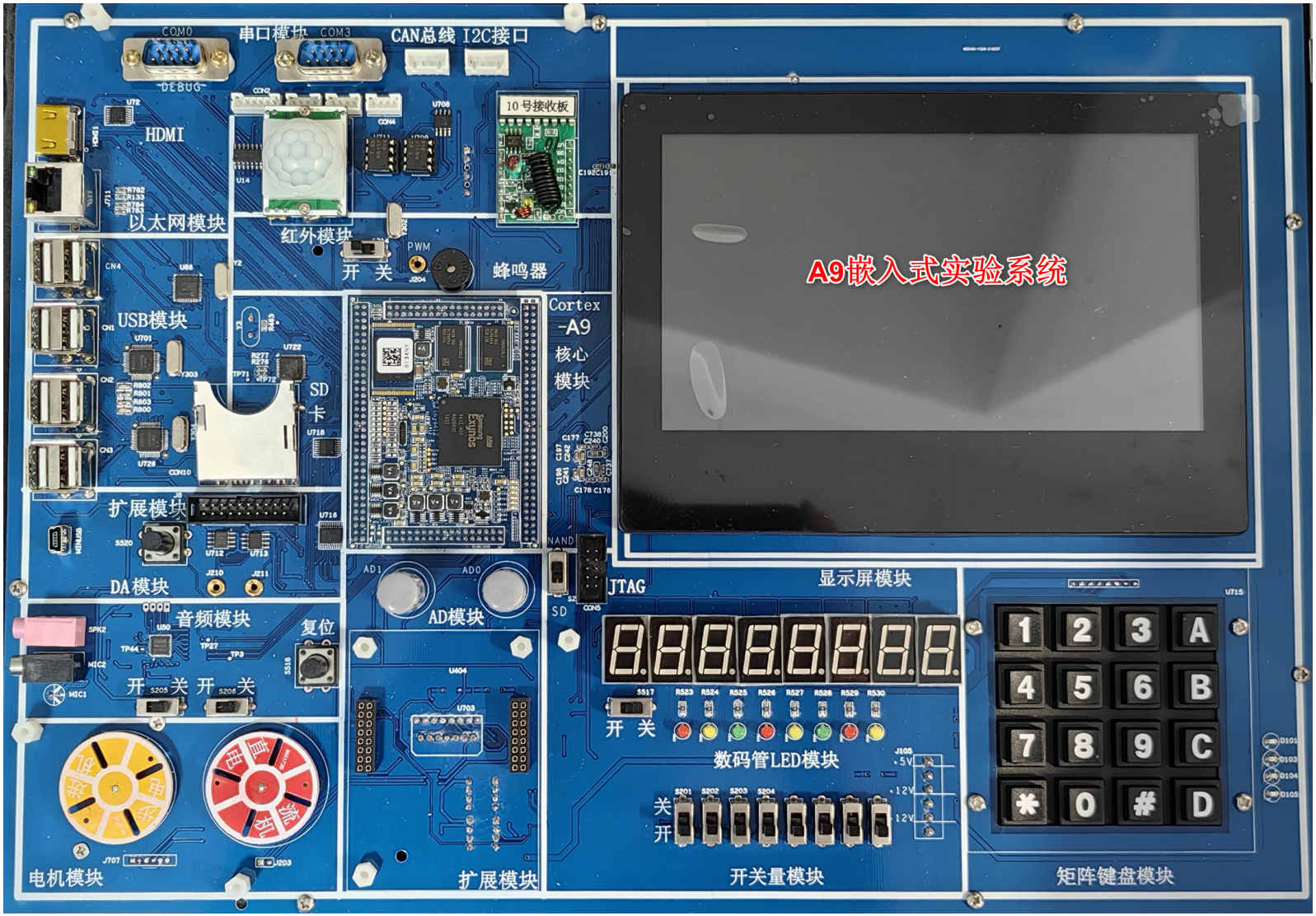
第5章 S5PV210处理器

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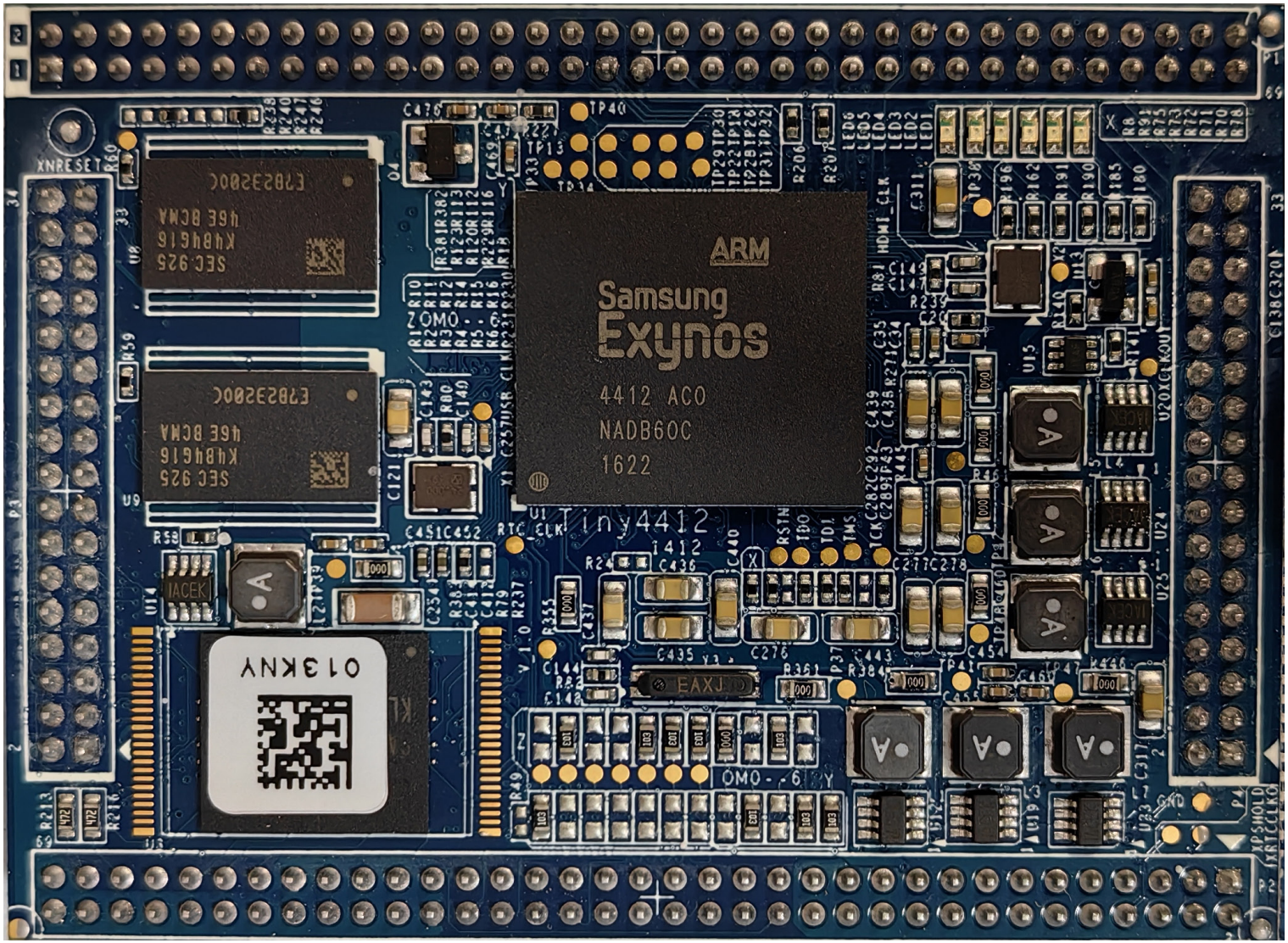
章节内容

- S5PV210处理器简介
- 时钟及电源管理单元
- 存储管理单元
- 中断控制器
- 通用I/O
- 串行通信单元
- 定时器单元
- 多媒体控制单元
- 移动通信接口

5.1 处理器简介


COM0
串口模块
COM3
CAN总线 I2C接口
DEBUG
HDMI
以太网模块
红外模块
10号接收板
开 关
PWM
蜂鸣器
A9嵌入式实验系统
USB模块
Cortex
-A9
核心
模块
SD
卡
扩展模块
DA模块
音频模块
复位
开 关 开 关
AD模块
JTAG
显示屏模块
开 关
数码管LED模块
关
开
开关量模块
1 2 3 A
4 5 6 B
7 8 9 C
* 0 # D
矩阵键盘模块
电机模块
扩展模块

5.1 处理器简介



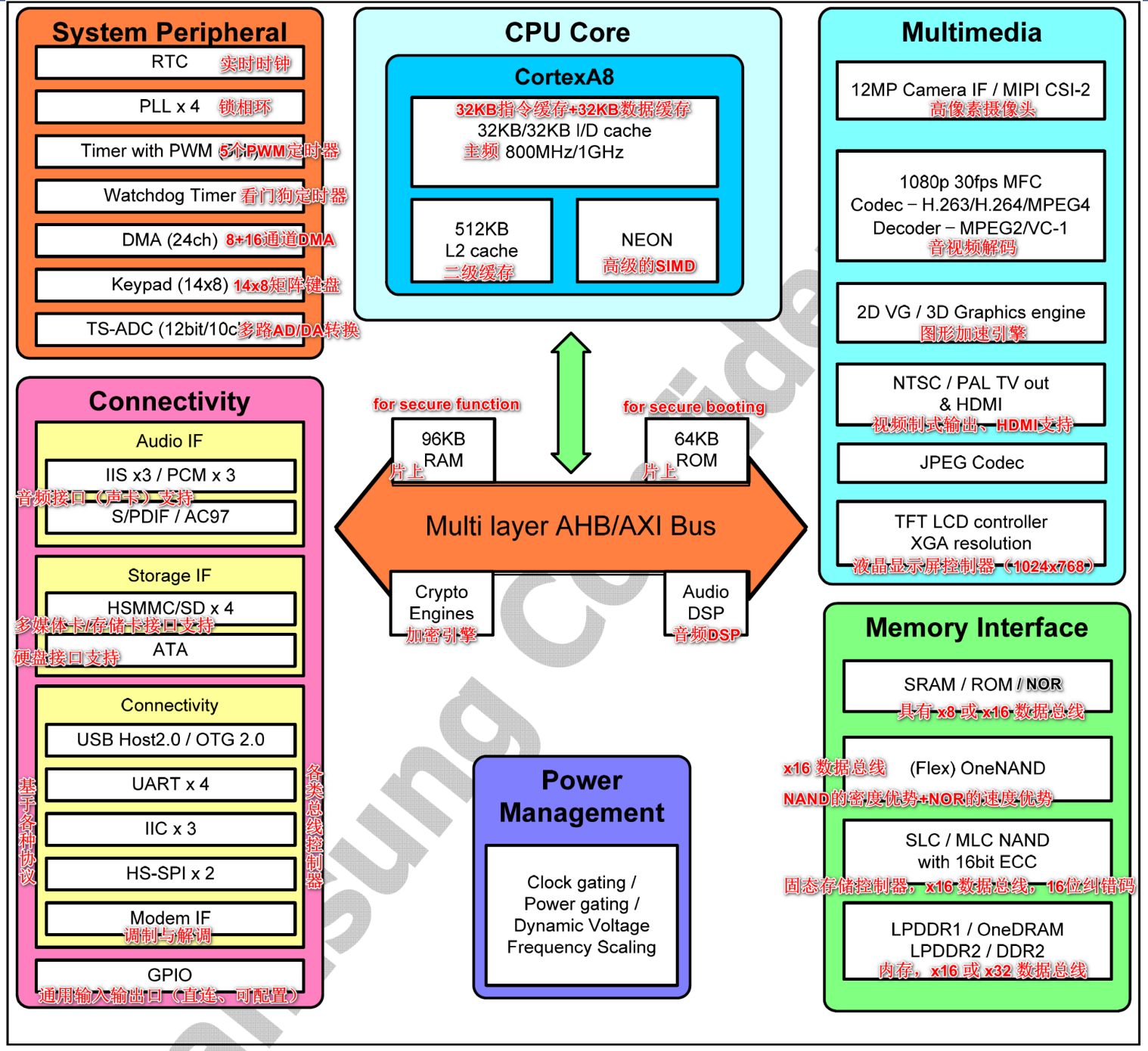


Figure 1-1 S5PV210 Block Diagram

Ref.: DataSheet P.29

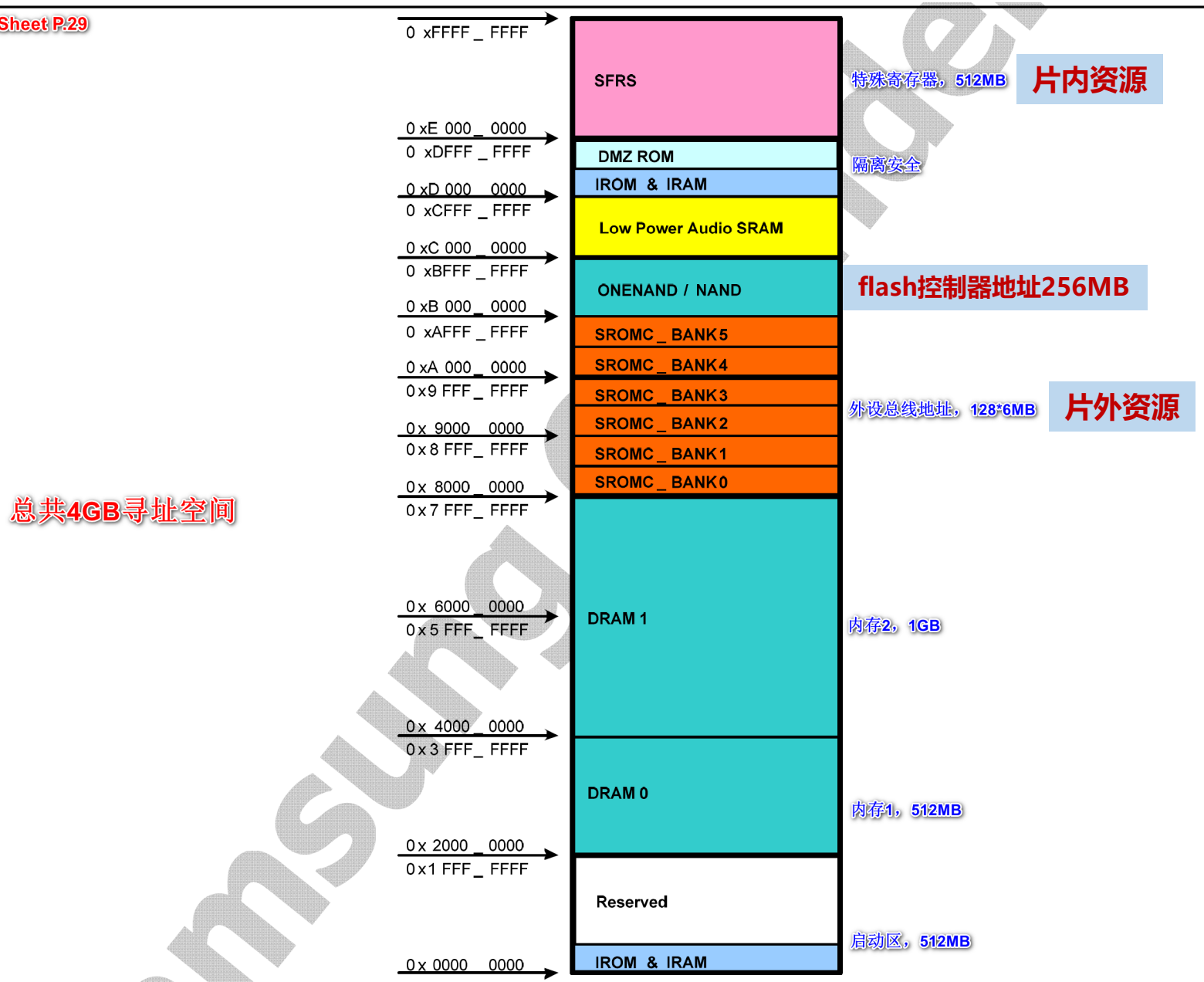


Figure 2-1 Address Map

2.1.1 DEVICE SPECIFIC ADDRESS SPACE

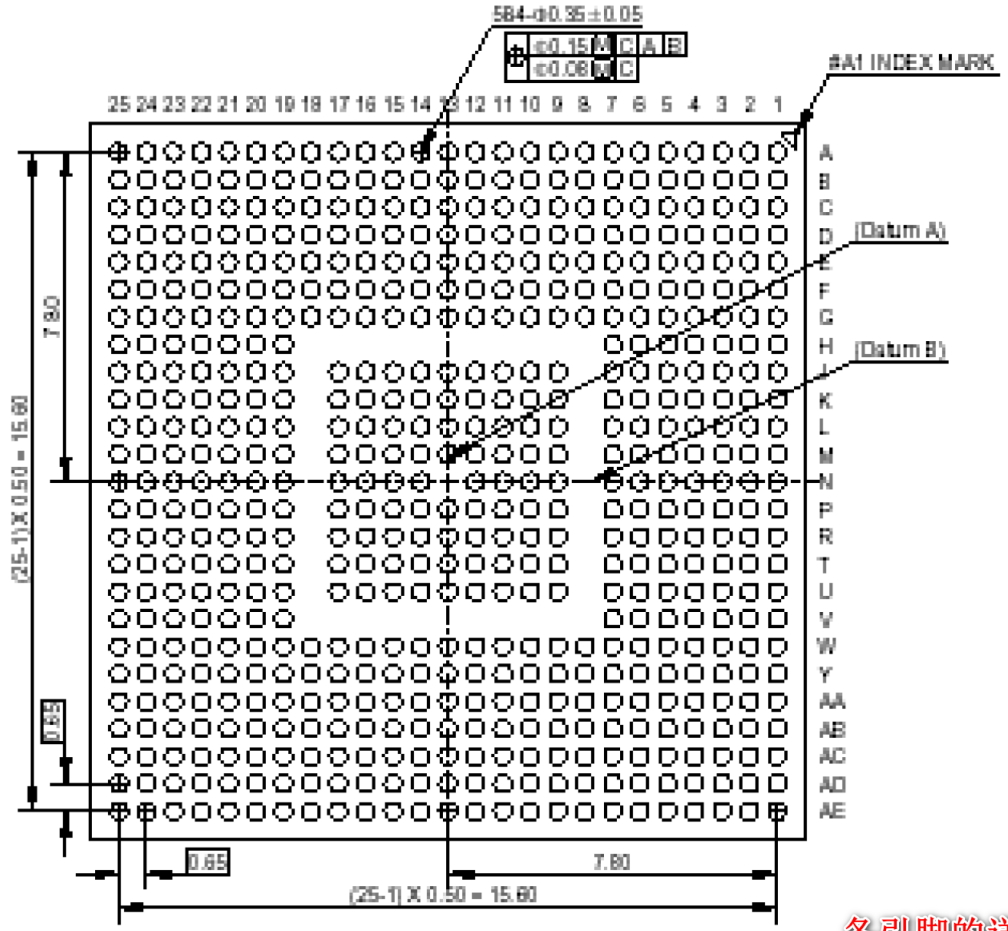
Address		Size	Description	Note
0x0000_0000	0x1FFF_FFFF	512MB	Boot area	Mirrored region depending on the boot mode.
0x2000_0000	0x3FFF_FFFF	512MB	DRAM 0	
0x4000_0000	0x7FFF_FFFF	1024MB	DRAM 1	
0x8000_0000	0x87FF_FFFF	128MB	SROM Bank 0	
0x8800_0000	0x8FFF_FFFF	128MB	SROM Bank 1	
0x9000_0000	0x97FF_FFFF	128MB	SROM Bank 2	
0x9800_0000	0x9FFF_FFFF	128MB	SROM Bank 3	
0xA000_0000	0xA7FF_FFFF	128MB	SROM Bank 4	
0xA800_0000	0xAFFF_FFFF	128MB	SROM Bank 5	
0xB000_0000	0xBFFF_FFFF	256MB	OneNAND/NAND Controller and SFR	
0xC000_0000	0xCFFF_FFFF	256MB	MP3_SRAM output buffer	
0xD000_0000	0xD000_FFFF	64KB	IROM	
0xD001_0000	0xD001_FFFF	64KB	Reserved	
0xD002_0000	0xD003_7FFF	96KB	IRAM	
0xD800_0000	0xDFFF_FFFF	128MB	DMZ ROM	
0xE000_0000	0xFFFF_FFFF	512MB	SFR region	

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2.1.2 SPECIAL FUNCTION REGISTER MAP

Address		Description
0xE000_0000	0xE00F_FFFF	CHIPID
0xE010_0000	0xE01F_FFFF	SYSCON
0xE020_0000	0xE02F_FFFF	GPIO
0xE030_0000	0xE03F_FFFF	AXI_DMA
0xE040_0000	0xE04F_FFFF	AXI_PSYS
0xE050_0000	0xE05F_FFFF	AXI_PSFR
0xE060_0000	0xE06F_FFFF	TZPC2
0xE070_0000	0xE07F_FFFF	IEM_APC
0xE080_0000	0xE08F_FFFF	IEM_IEC
0xE090_0000	0xE09F_FFFF	PDMA0
0xE0A0_0000	0xE0AF_FFFF	PDMA1
0xE0D0_0000	0xE0DF_FFFF	CORESIGHT
0xE0E0_0000	0xE0EF_FFFF	SECKEY
0xE0F0_0000	0xE0FF_FFFF	ASYNC_AUDIO_PSYS
0xE110_0000	0xE11F_FFFF	SPDIF
0xE120_0000	0xE12F_FFFF	PCM1
0xE130_0000	0xE13F_FFFF	SPI0
0xE140_0000	0xE14F_FFFF	SPI1
0xE160_0000	0xE16F_FFFF	KEYIF
0xE170_0000	0xE17F_FFFF	TSADC

3.1.1 PIN ASSIGNMENT DIAGRAM - 584-BALL FCFBGA 584个引脚



P. 47

各引脚的详细描述见Datasheet 3.2节

Figure 3-1 S5PV210 Pin Assignment (584-FCFBGA) Bottom View

5.1 处理器简介：启动顺序

- S5PV210 consists of 64KB ROM and 96KB SRAM as internal memory.
  - For booting, internal 64KB ROM and internal 96KB SRAM regions can be used.
  - S5PV210 boots from internal ROM to enable secure booting, which ensures that the image cannot be altered by unauthorized users.
  - To select secure booting or normal booting, S5PV210 should use e-fuse information. This information cannot be altered after being programmed.

5.1 处理器简介：启动顺序

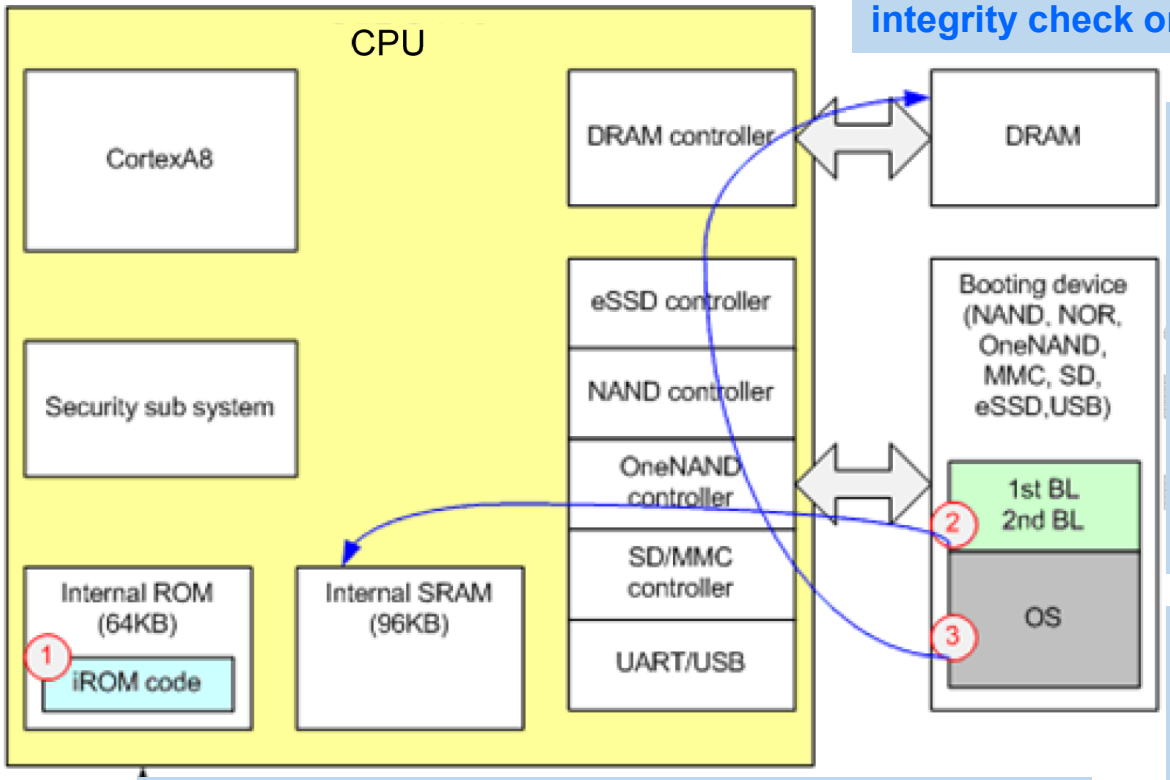
- The booting device can be chosen from following list:
  - General NAND Flash memory
  - OneNAND memory
  - SD/ MMC memory (such as MoviNAND and iNAND)
  - eMMC memory
  - eSSD memory
  - UART and USB devices
    - USB booting is provided for system debugging and flash reprogramming, not for normal booting.

5.1 处理器简介：启动顺序

- **The boot loader is largely composed of:**
  - **iROM code:**
    Contains small and simple code, which is platform-independent and stored in internal memory
  - **First boot loader:**
    Contains small and simple code, which is platform-independent and stored in external memory device. Related to secure booting.
  - **Second boot loader:**
    Contains complex code, which is platform-specific and stored in external memory device.

5.1 处理器简介：启动顺序

The second boot loader initializes system clock, UART, and DRAM controller. Then, it loads OS image from the booting device to DRAM. The second boot loader can do an integrity check on the OS image.



The first boot loader loads the second boot loader then may check the integrity of the second boot loader according the secure boot key values.

After the booting completes, the second boot loader jumps to the operating system.

三阶段具体操作内容参考手册521页

The iROM code is placed in internal 64KB ROM. It initializes basic system functions such as clock, stack, and heap.

The iROM loads the first boot loader image from a specific booting device to internal 96KB SRAM. The booting device is selected by Operating Mode (OM) pins. According to the secure boot key values, the iROM code may do an integrity check on the first boot loader image.

5.1 处理器简介：启动顺序

Table 6-1 Functions Needed for Various Reset Status

	Basic Initialization in iROM	PLL Setting in iROM	First Boot / Second Boot Loader Loading	DRAM Setting in Second Boot Loader	OS Loading	Restore Previous State
Hardware Reset	O	O	O	O	O	X
Watchdog Reset	O	O	O	O	O	X
Wake up from SLEEP	O	O	O	O	X	O
SW reset	O	O	O	O	O	X
Wake up from DEEP_STOP	O	X	X (note)	X	X	O
Wake up from DEEP_IDLE	O	X	X (note)	X	X	O

NOTE: When the contents of SRAM are preserved by retention option.

The restoring previous state function is required on wake up from SLEEP, DEEP_STOP, and DEEP_IDLE modes.

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5.2 时钟及电源管理单元

- 时钟生成器为CPU和外围设备提供所需的时钟信号，可通过S/W控制每个外围设备块提供或者断开时钟，减少电源消耗
  - ✧ 时钟控制逻辑能够产生设备所需的时钟信号
  - ✧ 电源管理6种模式：
    Normal、Deep-idle、Stop、Deep-trop、Sleep
- S5PV210 consists of three clock domains:
  - ① main system (MSYS)
  - ② display system (DSYS)
  - ③ peripheral system (PSYS)

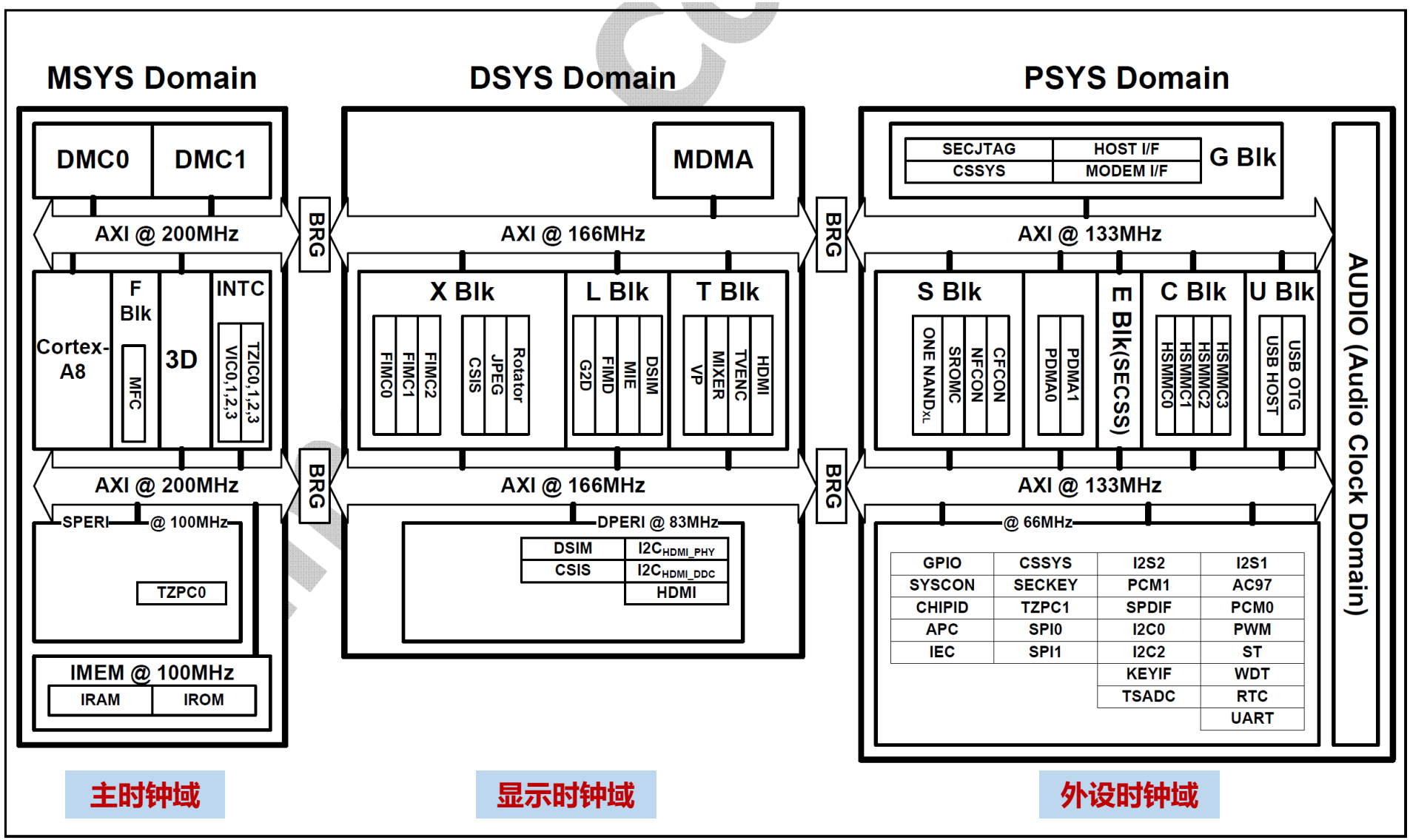


Figure 3-1 S5PV210 Clock Domains

5.2 时钟及电源管理单元

- System controller controls PLL, clock generator, the power management unit (PMU), and other system dependent units.
  - ✧ using Special Functional Register (SFR) within the system controller

3.7.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
APLL_LOCK	0xE010_0000	R/W	Control PLL locking period for APLL.	0x0000_0FFF
Reserved	0xE010_0004	-	Reserved	-
MPLL_LOCK	0xE010_0008	R/W	Control PLL locking period for MPLL.	0x0000_0FFF
Reserved	0xE010_000C	-	Reserved	-
EPLL_LOCK	0xE010_0010	R/W	Control PLL locking period for EPLL.	0x0000_0FFF
Reserved	0xE010_0014~	-	Reserved	-

Register	Address	R/W	Description	Reset Value
CLK_SRC0	0xE010_0200	R/W	Select clock source 0 (Main)	0x0000_0000
CLK_SRC1	0xE010_0204	R/W	Select clock source 1 (Multimedia)	0x0000_0000
CLK_SRC2	0xE010_0208	R/W	Select clock source 2 (Multimedia)	0x0000_0000
CLK_SRC3	0xE010_020C	R/W	Select clock source 3 (Multimedia)	0x0000_0000
CLK_SRC4	0xE010_0210	R/W	Select clock source 4 (Connectivity)	0x0000_0000
CLK_SRC5	0xE010_0214	R/W	Select clock source 5 (Connectivity)	0x0000_0000
CLK_SRC6	0xE010_0218	R/W	Select clock source 6 (Audio)	0x0000_0000
CLK_SRC_MASK0	0xE010_0280	R/W	Clock source mask 0	0xFFFF_FFFF
CLK_SRC_MASK1	0xE010_0284	R/W	Clock source mask 1	0xFFFF_FFFF

时钟源寄存器映射，共9个时钟源寄存器

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5.2 时钟及电源管理单元

- S5PV210 has many clock sources, which include four PLL outputs, the external oscillator, the external clock, and other clock sources from GPIO.
  - ✧ CLK_SRCn registers control the source clock of each clock divider. (Datasheet P.378)

5.3 中断控制器

- S5PV210的中断控制器组成：
  ① four Vectored Interrupt Controller (VIC)
  ② ARM PrimeCell PL192
  ③ four TrustZone Interrupt Controller (TZIC)
  ④ SP890

5.3 中断控制器

- **VIC的关键特性：**
  - Supports 93 vectored IRQ interrupts 93个IRQ中断源
  - Fixed hardware interrupts priority levels
  - Programmable interrupt priority levels
  - Supports Hardware interrupt priority level masking
  - Programmable interrupt priority level masking
  - Generates IRQ and FIQ
  - Generates Software interrupt
  - Test registers
  - Raw interrupt status
  - Interrupt request status
  - Supports Privileged mode for restricted access

5.3 中断控制器

- **VIC的关键特性：**
  - VIC有四个组（VIC3~VIC0），每组均包含有32个中断源，合计128个中断源（有一些是空的）
  - 所支持的中断源，从GPIO的EINT（中断使能）到UART等各类通讯总线再到多媒体信号等，利用好向量中断控制器，才能更加高效地使用CPU的计算资源，服务于具体的工作需求
  - 参考中断源表 **Datasheet P.560**

VIC1端口号 31~0

中断编号 127~0

中断请求

Module	VIC port no	No	INT Request	Remark
Connectivity, Storage **ARM, power, memory**	26	58	HSMMC0	
	25	57	MODEMIF	
	24	56	OTG (usb)	
	23	55	UHOST (usb)	
	22	54		
	21	53		
	20	52	I2C_HDMI_PHY	
	19	51	I2C2	
	18	50	AUDIO_SS	
	17	49		
	16	48	SPI1	
	15	47	SPI0	
	14	46	I2C0	
	13	45	UART3	
	12	44	UART2	
	11	43	UART1	
	10	42	UART0	
	9	41	CFC	
	8	40	NFC	

举例：VIC1（部分）

寄存器映射地址：对应相应寄存器实现读取（状态）或控制（中断使能、清除、优先级设置等）

1.4.1 REGISTER MAP

Register	Address	R/W	Description	Reset Value
VIC0IRQSTATUS	0xF200_0000	R	Specifies the IRQ Status Register	0x00000000
VIC0FIQSTATUS	0xF200_0004	R	Specifies the FIQ Status Register	0x00000000
VIC0RAWINTR	0xF200_0008	R	Specifies the Raw Interrupt Status Register	-
VIC0INTSELECT	0xF200_000C	R/W	Specifies the Interrupt Select Register	0x00000000
VIC0INTENABLE	0xF200_0010	R/W	Specifies the Interrupt Enable Register	0x00000000
VIC0INTENCLEAR	0xF200_0014	W	Specifies the Interrupt Enable Clear Register	-
VIC0SOFTINT	0xF200_0018	R/W	Specifies the Software Interrupt Register	0x00000000
VIC0SOFTINTCLEAR	0xF200_001C	W	Specifies the Software Interrupt Clear Register	-
VIC0PROTECTION	0xF200_0020	R/W	Specifies the Protection Enable Register	0x0
VIC0SWPRIORITYMASK	0xF200_0024	R/W	Software Priority Mask Register	0xFFFF
VIC0PRIORITYDAISY	0xF200_0028	R/W	Specifies the Vector Priority Register for Daisy Chain	0xF
VIC0VECTADDR0	0xF200_0100	R/W	Specifies the Vector Address 0 Register	0x00000000
VIC0VECTADDR1	0xF200_0104	R/W	Specifies the Vector Address 1 Register	0x00000000
VIC0VECTADDR2	0xF200_0108	R/W	Specifies the Vector Address 2 Register	0x00000000

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5.4 存储控制器

- 主要有5类：
  - DRAM 控制器
  - SROM 控制器
  - OneNAND 控制器
  - NAND Flash 控制器
  - Compact Flash 控制器
  - 外部总线接口（EBI）

5.4 存储控制器：DRAM控制器

- S5PV210 has two independent DRAM Controllers and Ports, namely, DMC0 and DMC1.
  - DMC0 support maximum 512MByte memory size.
  - DMC1 support maximum 1GByte memory size.
  - Both controllers must use the memory of the same type.
- 关键特性
  - 兼容 DDR2, LPDDR, LPDDR2 多规格 SDRAM
  - 使用 SEC LPDDR2 PHY 接口支持高速存储设备
  - 支持 128 Mb, 256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb density 存储设备
  - 支持 16 / 32-bit 存储数据位宽
  - 优化保证低延迟的流水线技术
  - ……

5.4 存储控制器：DRAM控制器

1.3 I/O DESCRIPTION

Signal	I/O	Description	PAD	Type
DDR2SEL	I	Memory Type Selection (0: LPDDR1, 1: DDR2, LPDDR2)	XDDR2SEL	dedicated
SCLK	O	Memory Clock	Xm1(2)SCLK	dedicated
nSCLK	O	Memory Negative Clock	Xm1(2)nSCLK	dedicated
RASn	O	Row Address Selection	Xm1(2)RASn	dedicated
CASn	O	Column Address Selection	Xm1(2)CASn	dedicated
WEn	O	Write Enable	Xm1(2)WEn	dedicated
DATA[31:0]	I/O	Memory Data Bus	Xm1(2)DATA[31:0]	dedicated
DQM[3:0]	O	Write Masking Per Byte	Xm1(2)DQM[3:0]	dedicated
DQSp[3:0]	I/O	Data Strobe Signal Per Byte	Xm1(2)DQS[3:0]	dedicated
DQSn[3:0]	I/O	Data Strobe Negative Signal Per Byte	Xm1(2)DQSn[3:0]	dedicated
ADDR[15:0]	O	Memory Address, Bank Address	Xm1(2)ADDR[15:0]	dedicated
CSn[1:0],	O	Memory CS signals	Xm1(2)CSn[1:0]	dedicated
CKE[1:0]	O	Memory CKE signals	Xm1(2)CKE[1:0]	dedicated

数据选通DS

片选CS

时钟使能CKE

~DRAM引脚

SoC 引脚

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1.4 REGISTER DESCRIPTION

1.4.1 REGISTER MAP 寄存器映射地址

Register	Address	R/W	Description	Reset Value
DMC0				
CONCONTROL	0xF000_0000	R/W	Specifies the Controller Control Register	0x0FFF_1350
MEMCONTROL	0xF000_0004	R/W	Specifies the Memory Control Register	0x0020_2100
MEMCONFIG0	0xF000_0008	R/W	Specifies the Memory Chip0 Configuration Register	0x20F0_0312
MEMCONFIG1	0xF000_000C	R/W	Specifies the Memory Chip1 Configuration Register	0x30F0_0312
DIRECTCMD	0xF000_0010	R/W	Specifies the Memory Direct Command Register	0x0000_0000
PRECHCONFIG	0xF000_0014	R/W	Specifies the Precharge Policy Configuration Register	0xFF00_0000
PHYCONTROL0	0xF000_0018	R/W	Specifies the PHY Control0 Register	0x0000_0000
PHYCONTROL1	0xF000_001C	R/W	Specifies the PHY Control1 Register	0x0000_0040
RESERVED	0xF000_0020	R	Reserved	0x0000_0000
PWRDNCONFIG	0xF000_0028	R/W	Specifies the Dynamic Power Down Configuration Register	0xFFFF_00FF
TIMINGAREF	0xF000_0030	R/W	Specifies the AC Timing Register for SDRAM Auto Refresh	0x0000_040E
TIMINGROW	0xF000_0034	R/W	Specifies the AC Timing Register for SDRAM Row	0x0F23_3286
TIMINGDATA	0xF000_0038	R/W	Specifies the AC Timing Register for SDRAM Data	0x1213_0204

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1.4.1.2 Memory Control Register (MemControl, R/W, Address = 0xF000_0004, 0xF140_0004)

MEMCONTROL	Bit	Description	R/W	Initial State
Reserved	[31:23]	Should be zero		0x0
bl	[22:20]	Memory Burst Length 0x0 = Reserved 0x1 = 2 0x2 = 4 0x3 = 8 0x4 = 16 0x5 ~ 0x7 = Reserved In case of DDR2/ LPDDR2, the controller only supports burst length 4.	R/W	0x2
num_chip	[19:16]	Number of Memory chips 0x0 = 1 chip 0x1 = 2 chips 0x2 ~ 0xf = Reserved	R/W	0x0
mem_width	[15:12]	Width of Memory Data Bus 0x0 = Reserved 0x1 = 16-bit 0x2 = 32-bit 0x3 ~ 0xf = Reserved	R/W	0x2
mem_type	[11:8]	Type of Memory 0x0 = Reserved 0x1 = LPDDR	R/W	0x1

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5.4 存储控制器：SROM控制器

- SROM是与CPU连接时，采用总线式的访问方法
  SROM BANK就是SoC提供的对外总线式连接SRAM/ROM的接口
- S5PV210 SROM Controller (SROMC) support external 8 / 16-bit NOR Flash/ PROM/ SRAM memory.
- 关键特性
  - 支持 SRAM, various ROMs, NOR flash memory (如网卡芯片也可以)
  - 只支持 8/16-bit 数据总线 (only 16-bit for BANK0)
  - 支持 6 banks：BANK5~BANK0
  - 固定 BANK 的起始地址
  - 利用 External wait 扩展总线周期
  - 支持外部存储器的字节和半字访问

5.4 存储控制器：SROM控制器

2.3 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
nGCS[5:0]	Output	Bank selection signal	Xm0CSn[5:0]	muxed
ADDR[22:0]	Output	SROM Address bus	Xm0ADDR[22:0]	muxed
nOE	Output	SROM Output Enable	Xm0OEn	muxed
nWE	Output	SROM Write Enable	Xm0WEn	muxed
nWBE/nBE [1:0]	Output	SROM Byte write Enable / Byte Enable	Xm0BEn	muxed
DATA[15:0]	In/Out	SROM Data bus	Xm0DATA[15:0]	muxed
nWAIT	Input	SROM Wait input	Xm0WAITn	muxed

SoC 引脚

- 寄存器映射、寄存器描述，参考：**Datasheet P.647**

5.4 存储控制器：OneNAND控制器

- **S5PV210 supports external 16-bit bus for OneNAND and Flex-OneNAND memory devices.**
  - ✧ 支持异步和同步读/写总线操作
  - ✧ 集成专用的 DMA engine 加速 OneNAND存储设备的运行

5.4 存储控制器：NAND Flash控制器

- 替代 Nor flash 的执行方式：
  - ① The boot code in S5PV210 can be executed on external NAND flash.
  - ② It will copy NAND flash data to DRAM.
  - ③ To validate the NAND flash data, S5PV210 comprises of hardware Error Correction Code (ECC).
  - ④ After the NAND flash content is copied to DRAM, main program will be executed on DRAM.

5.4 存储控制器：NAND Flash控制器

- 关键特性：
  - 支持 512Bytes, 2KB, 4KB, 8KB 页尺寸（MMU中的页）
  - 可以直接访问 NAND flash 进行读写等
  - 支持 8-bit NAND flash 接口总线
  - 硬件纠错码（ECC）
  - 支持 SLC 和 MLC 类型的 NAND
  - 支持“字节/半字/字”的方式访问数据和ECC数据寄存器，以“字”访问其他寄存器

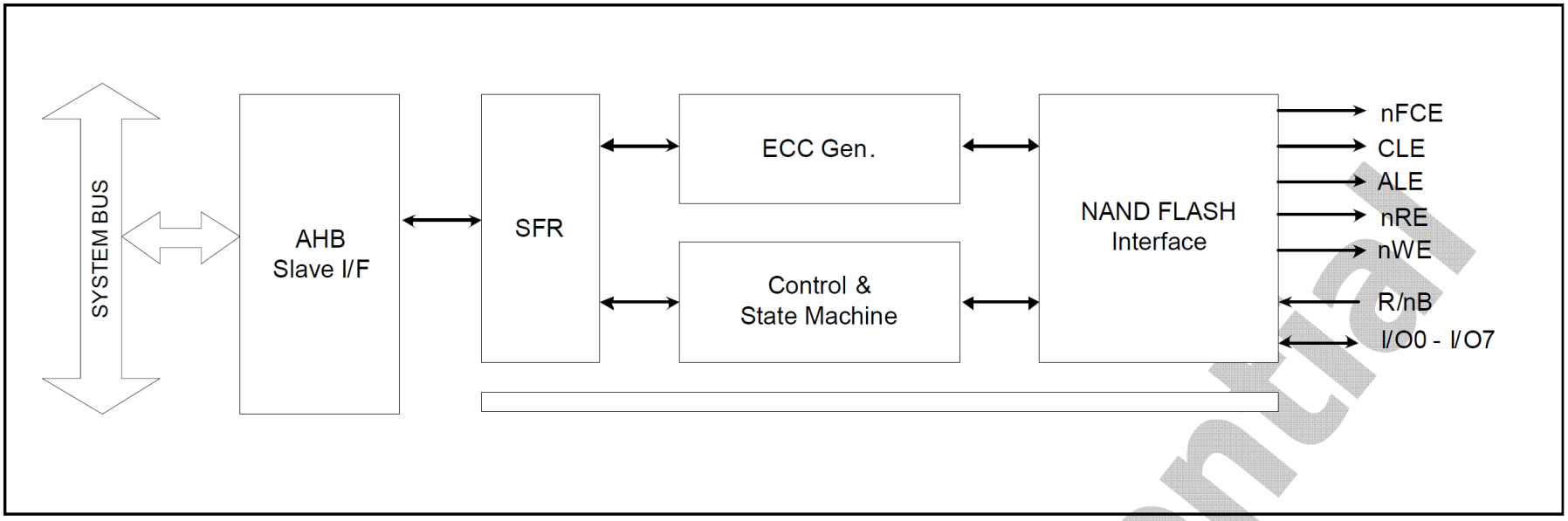


Figure 4-1 NAND Flash Controller Block Diagram

4.4 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
Xm0DATA	Input / Output	Address / Data Bus	Xm0DATA	muxed
Xm0FRnB[3:0]	Input	Ready and Busy	Xm0FRnB	muxed
Xm0FCLE	Output	Command Latch Enable	Xm0FCLE	muxed
Xm0FALE	Output	Address Latch Enable	Xm0FALE	muxed
Xm0CSn[2:5]	Output	Chip Enable 地址锁存使能	Xm0CSn	muxed
Xm0FREn	Output	Read Enable	Xm0FREn	muxed
Xm0FWEn	Output	Write Enable	Xm0FWEn	muxed

- 寄存器映射、寄存器描述，参考：**Datasheet P.706**

5.4 存储控制器：Compact Flash 控制器

- The Compact Flash Controller (CFC) can control the Hard Disk and the Compact Flash that can operate in true IDE mode. （存储控制器与存储器集成在一起——compact）
- 关键特性：
  - Supports all ATA PIO from mode 0 to mode 4.
  - Supports Multi-Word DMA (MDMA) from mode 0 to mode 2.
  - Supports Ultra DMA (UDMA) from mode 0 to mode 4.
  - Connects up to two devices.

5.4 存储控制器：Compact Flash 控制器

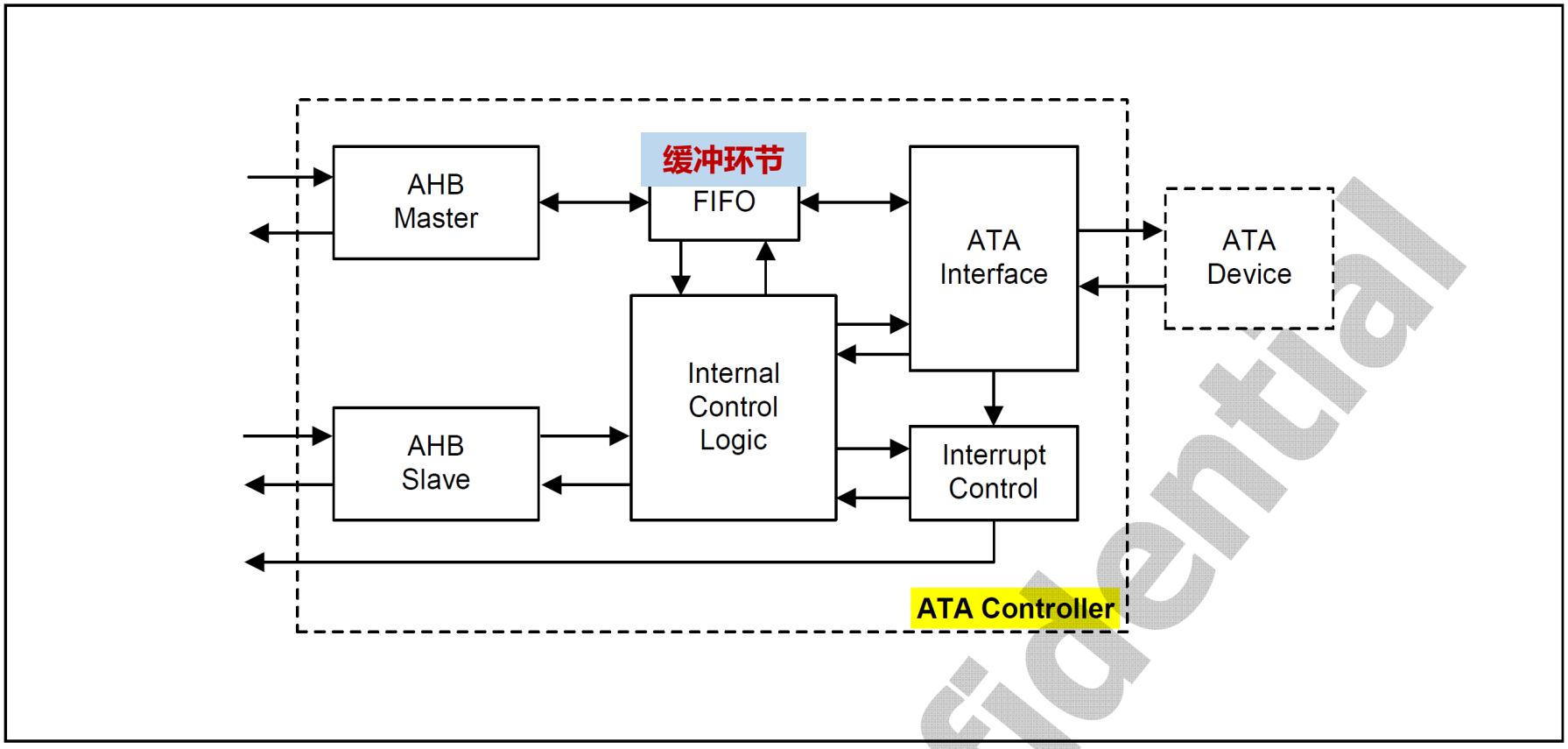


Figure 5-1 Block Diagram of Compact Flash Controller

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5.10 I/O DESCRIPTION

Signal	I/O	Description	Pad	Type
CSn0	O	Device chip selection signal To select the control block registers	XmsmCSn	muxed
CSn1	O	Device chip selection signal To select the command block registers	XmsmWEn	muxed
DA[2:0]	O	register address signals	XmsmADDR[2:0]	muxed
DD_RD[15:0]	I	Read Data Bus	XmsmDATA[15:0]	muxed
DD_WR[15:0]	O	Write Data Bus	XmsmDATA[15:0]	muxed
DD_wr_en	O	Data Output Enable Strobe		
IORDY	I	Data transfer wait signal. DMA ready during UDMA write. DMA strobe during UDMA read.	XmsmADDR[3]	muxed
INTRQ	I	Device Interrupt signal.	XmsmADDR[4]	muxed
DMARQ	I	The DMA request signal for data transfers between host and device.	XmsmADDR[5]	muxed
DRESETn	O	Device reset signal from host.	XmsmADDR[6]	muxed
DMACKn	O	The DMA acknowledge signal that data has been accepted or data is available.	XmsmADDR[7]	muxed
DIORn (HDMA_RDYn,	O	IO Read Enable Strobe. DMA ready during UDMA read.	XmsmRn	muxed

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- 寄存器映射、寄存器描述，参考：**Datasheet P.737**

5.5 直接存储器访问控制器（DMAC）

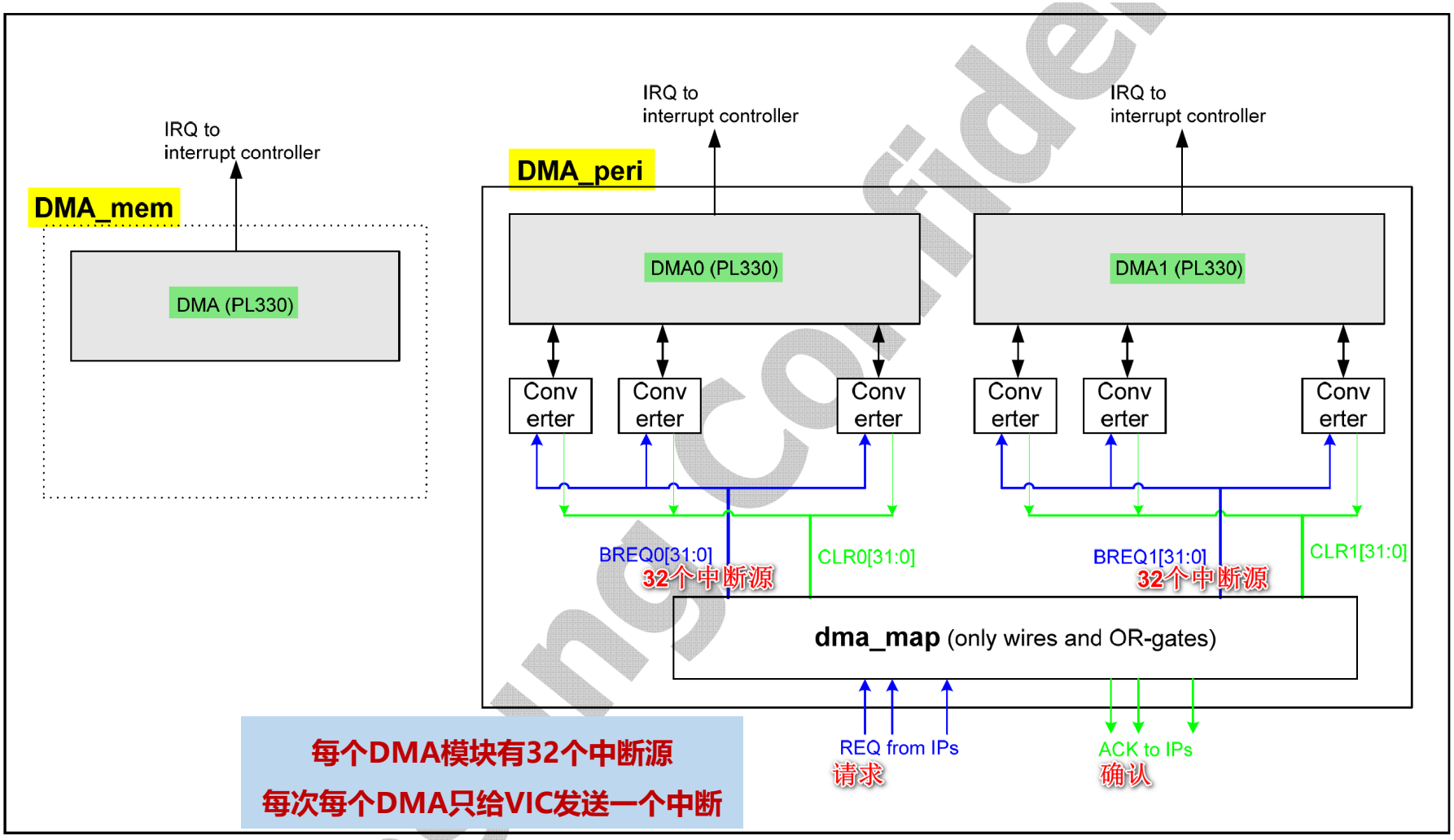


Figure 1-1 Two DMA Tops

1.1.1 KEY FEATURES OF DMA CONTROLLER

The key features of DMA Controller are listed below as reference for DMA and for writing DMA assembly code.

Key Features	DMA_mem	DMA_peri
Supports Data Size	Up to double word (64-bit)	Up to word (32-bit)
Supports Burst Size	Up to 16 burst	Word transfer: Up to 8 burst
		Byte or word transfer: Up to 16 burst
Supports Channel	8 channels at the same time	16 channels at the same time

Although each DMA module has 32 interrupt sources, only one interrupt is sent to Vectored Interrupt Controller (VIC) for each DMA. To see the interrupt number of DMA, refer to the interrupt number table in Chapter, “04.01.Interrupt Controller”. The software reads Interrupt Status (INTSTATUS) register for each module to check whether an interrupt occurs.

Table 1-1 DMA Request Mapping Table

Module	中断号 No.	DMA Request	Category	Service Module
Peri DMA1	31	PCM2_TX	Audio	by only DMA1
	30	PCM2_RX		
	29	MSM_REQ3	Others	
	28	MSM_REQ2		
	27	MSM_REQ1		

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Ref. Datasheet P.758

5.5 直接存储器访问控制器（DMAC）

- **关于寄存器：**
  - ✧ 大部分特殊功能寄存器（SFRs）为只读
  - ✧ 这些SFR主要用来检查PL330的状态
  - ✧ PL330有许多自己的SFRs
  - ✧ PL330有自己的**指令集**，参考Datasheet P.781
  - ✧ 通道控制寄存器和配置寄存器，参考Datasheet P.773

1.2.1. DMA_mem 的通道控制寄存器 (CC, R)

- CC_0, R, Address = 0xFA20_0408
- CC_1, R, Address = 0xFA20_0428
- CC_2, R, Address = 0xFA20_0448
- CC_3, R, Address = 0xFA20_0468
- CC_4, R, Address = 0xFA20_0488
- CC_5, R, Address = 0xFA20_04A8
- CC_6, R, Address = 0xFA20_04C8
- CC_7, R, Address = 0xFA20_04E8

8通道

CCn	Bit	Description	Initial State
dst_burst_size	[17:15]	Programs the burst size that DMAC uses when it writes the destination data. b000 = 1 byte b001 = 2 bytes b010 = 4 bytes b011 = 8 bytes Other = Reserved	0
src_burst_size	[3:1]	Programs the burst size that DMAC uses when it reads the source data. b000 = 1 byte b001 = 2 bytes b010 = 4 bytes	0

设置写目标数据的 burst size

设置写源数据的 burst size

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5.6 定时器（Timer）

- PWM 定时器
- 系统定时器
- 看门狗定时器
- 实时时钟（RTC）

5.6 定时器：PWM定时器

- S5PV210 有 5 个 32-bit PWM 定时器，用于产生 ARM 内部中断
  - 定时器 0, 1, 2, 3 均有一个 PWM 函数, 可以驱动外部 I/O 信号
  - 定时器 0 有一个可选的死区发生器，用于支持大电流设备
  - 定时器 4 仅作为内部定时器，没有输出引脚

- I/O描述，寄存器映射、寄存器描述，参考：Datasheet P.803

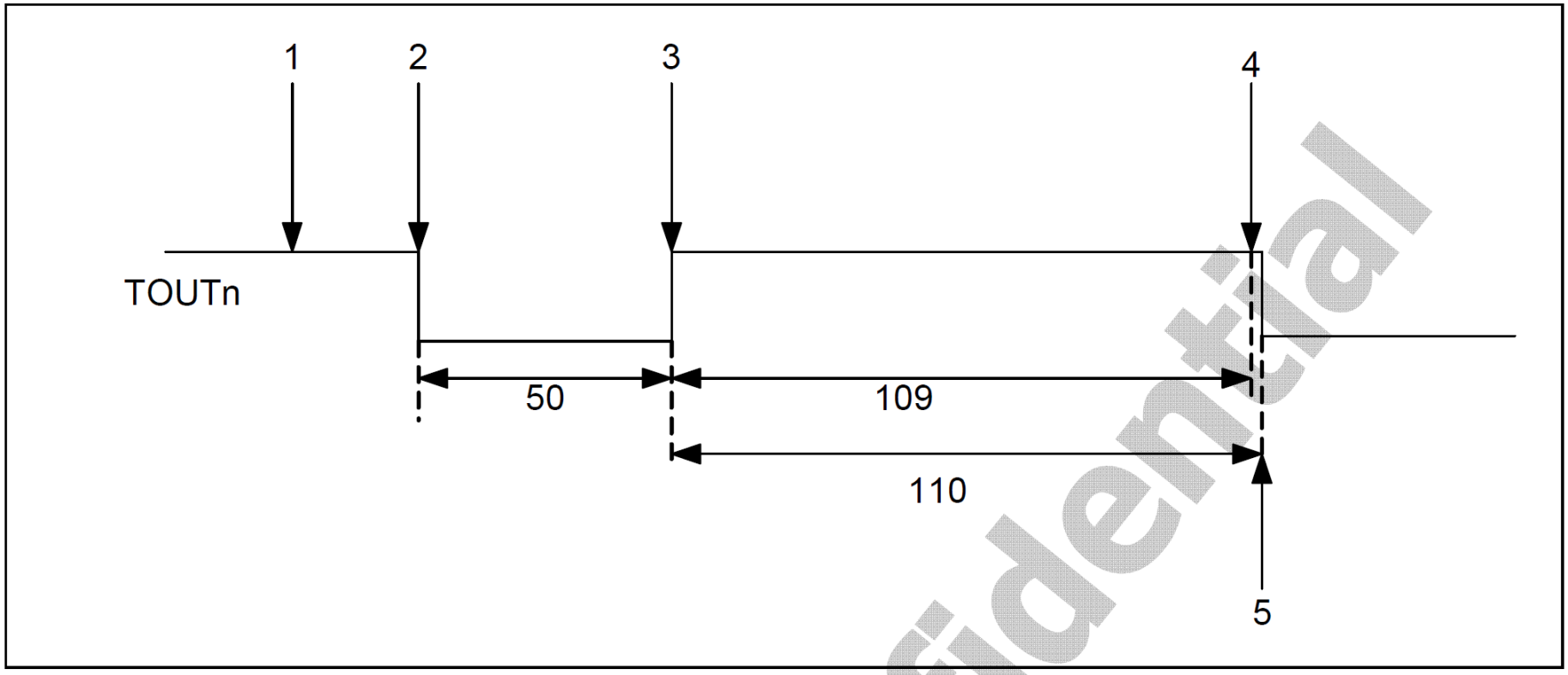


Figure 1-1 Simple Example of a PWM Cycle

Steps in PWM cycle:

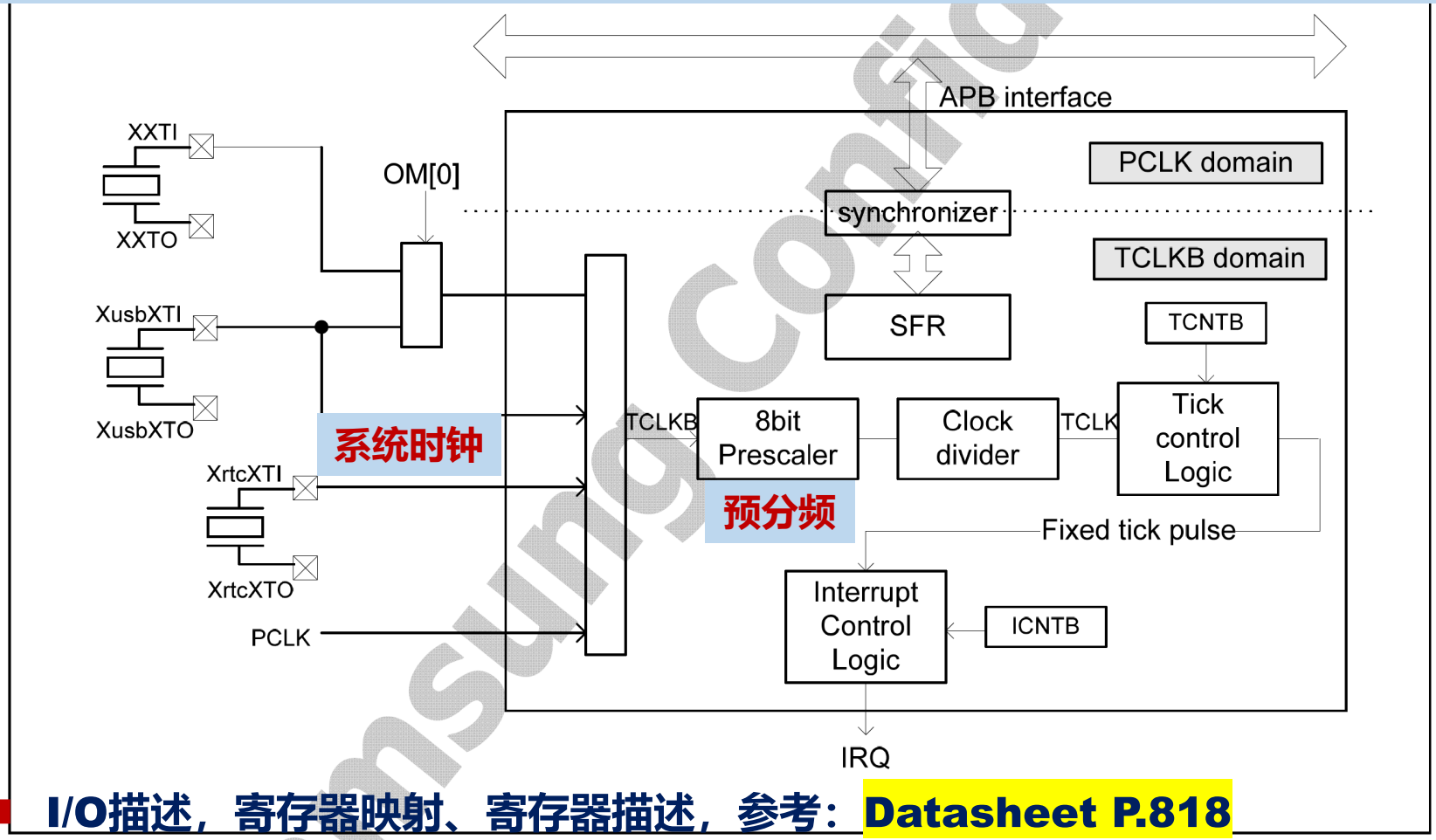
定时器缓冲寄存器 定时比较寄存器

- Initialize the TCNTBn register with 159(50+109) and TCMPBn with 109.
- Start Timer: Set the start bit and manually update this bit to off.
  The TCNTBn value of 159 is loaded into the down-counter, and then the output TOUTn is set to low.
- If down-counter counts down the value from TCNTBn to value in the TCMPBn register 109, the output changes from low to high
- If the down-counter reaches 0, it generates an interrupt request.
- The down-counter automatically reloads TCNTBn. This restarts the cycle.

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5.6 定时器：系统定时器

1. It provides 1ms time tick at any power mode except sleep mode.
2. Changeable interrupt interval without stopping reference tick timer.



I/O描述，寄存器映射、寄存器描述，参考：Datasheet P.818

Figure 2-1 Overall System Timer Block Diagram

5.6 定时器：看门狗定时器

- The Watchdog Timer (WDT) in S5PV210 is a timing device that resumes the controller operation after malfunctioning due to noise and system errors.
- The difference between WDT and PWM timer is that WDT generates the reset signal.

5.6 定时器：实时时钟（RTC）

- **RTC 为系统提供时间基准，在断电时可切换至备用电池**
  - ✧ **备用电池可以存储时间：秒，分，时，星期，日，月，年**
  - ✧ **RTC 工作频率为外部 32.768 kHz 晶振**

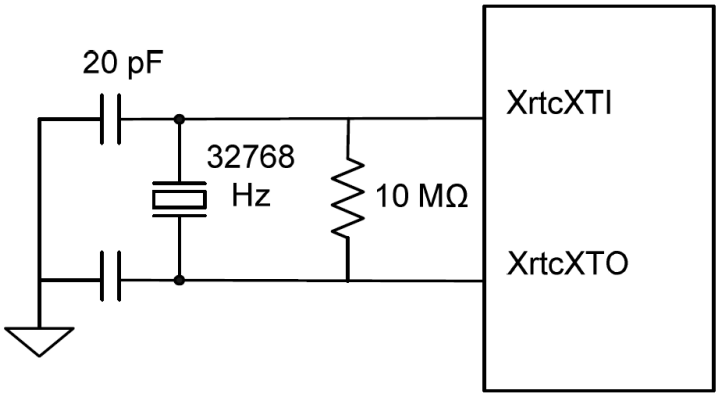


Figure 4-2 Main Oscillator Circuit Example

5.7 串行通信单元

- UART
- IIC
- SPI
- USB HOST
- USB OTG

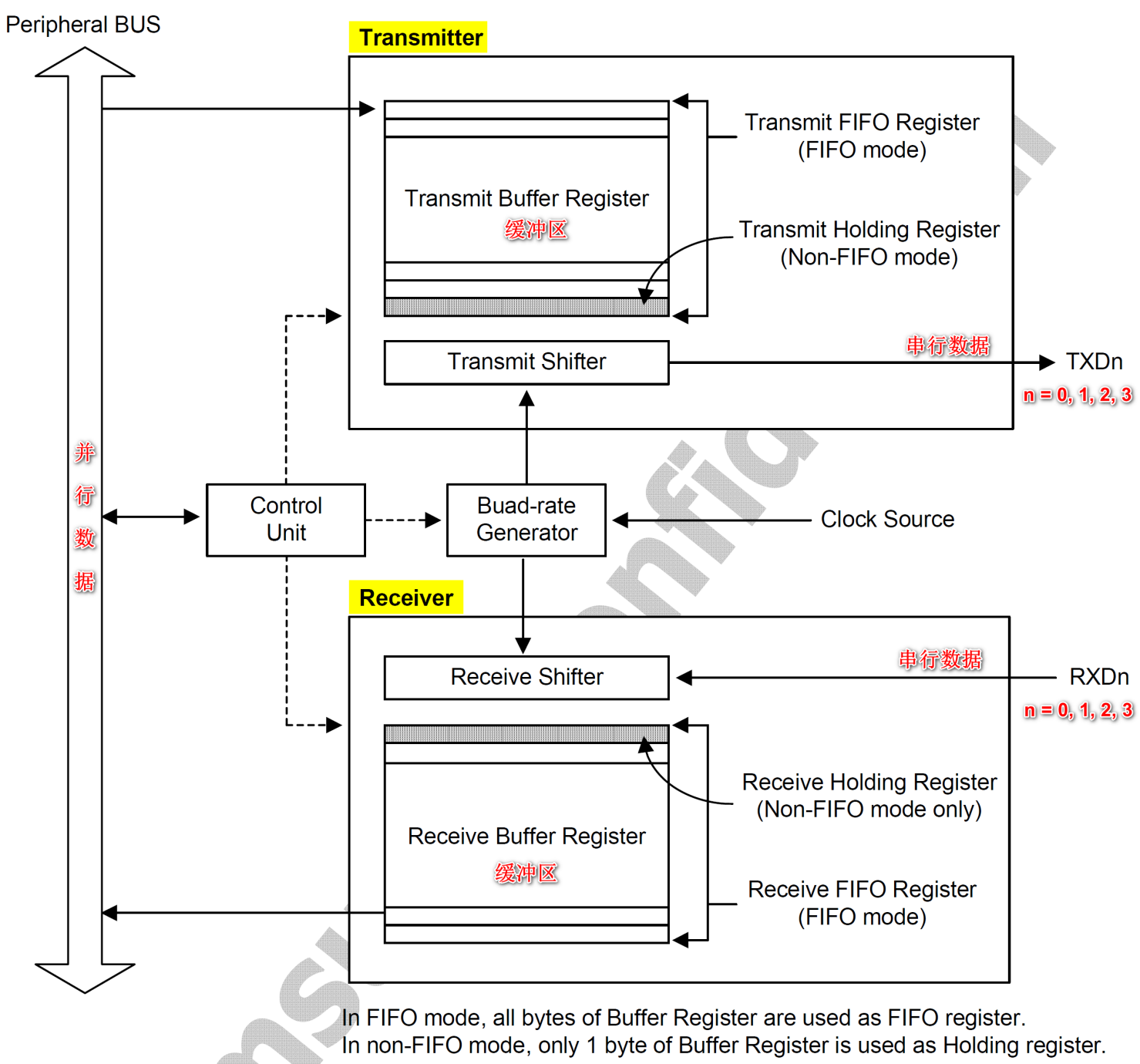
5.7 串行通信单元：UART

- **S5PV210提供 4 对独立的异步串行I/O端口，有 4 个独立通道**
  每个通道运行于 interrupt-based 或者 DMA-based 模式

Signal	I/O	Description	Pad	Type
UART_0_RXD	Input	Receives Data for UART0	XuRXD[0]	muxed
UART_0_TXD	Output	Transmits Data for UART0	XuTXD[0]	muxed
UART_0_CTSn	Input	Clears to Send(active low) for UART0	XuCTSn[0]	muxed
UART_0_RTSn	Output	Requests to Send(active low) for UART0	XuRTSn[0]	muxed
UART_1_RXD	Input	Receives Data for UART1	XuRXD[1]	muxed
UART_1_TXD	Output	Transmits Data for UART1	XuTXD[1]	muxed
UART_1_CTSn	Input	Clears to Send(active low) for UART1	XuCTSn[1]	muxed
UART_1_RTSn	Output	Requests to Send(active low) for UART1	XuRTSn[1]	muxed
UART_2_RXD	Input	Receives Data for UART2	XuRXD[2]	muxed
UART_2_TXD	Output	Transmits Data for UART2	XuTXD[2]	muxed
UART_2_CTSn	Input	Clears to Send(active low) for UART2	XuRXD[3]	muxed
UART_2_RTSn	Output	Requests to Send(active low) for UART2	XuTXD[3]	muxed
UART_3_RXD	Input	Receives Data for UART3	XuRXD[3]	muxed
UART_3_TXD	Output	Transmits Data for UART3	XuTXD[3]	muxed

NOTE: Type field indicates whether pads are dedicated to the signal or pads are connected to the multiplexed signals. UART external pads are shared with IrDA. In order to use these pads, GPIO must be set before the start of UART. Please refer to Section 2-2 GPIO for exact settings

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In FIFO mode, all bytes of Buffer Register are used as FIFO register.
In non-FIFO mode, only 1 byte of Buffer Register is used as Holding register.

Figure 1-1 Block Diagram of UART

1.6.1.1 UART Line Control Register

- ULCON0, R/W, Address = 0xE290_0000
- ULCON1, R/W, Address = 0xE290_0400
- ULCON2, R/W, Address = 0xE290_0800
- ULCON3, R/W, Address = 0xE290_0C00

There are four UART line control registers in the UART block, namely, ULCON0, ULCON1, ULCON2, and ULCON3.

ULCONn	Bit	Description	Initial State
Reserved	[31:7]	Reserved	0
Infrared Mode 红外模式	[6]	Determines whether to use the Infrared mode. 0 = Normal mode operation 1 = Infrared Tx/Rx mode	0
Parity Mode 奇偶校验模式	[5:3]	Specifies the type of parity generation to be performed and checking during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/ checked as 1 111 = Parity forced/ checked as 0	000
Number of Stop Bit	[2]	Specifies how many stop bits are used to signal end-of-frame signal. 0 = One stop bit per frame 1 = Two stop bit per frame	0

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■ 寄存器映射、寄存器描述参考：**Datasheet P.864**

5.7 串行通信单元：IIC总线

- S5PV210提供 4 个多主控 IIC 总线串行接口
- 通过专用双向串行数据线（SDA）和串行时钟线（SCL）在总线主控和连接在IIC总线上的设备之间进行通信——用于连接元件
- 控制多主控 IIC 总线时，需要写如下 4 个寄存器：
  ① Multi-master I2C-bus control register—I2CCON
  ② Multi-master I2C-bus control/status register—I2CSTAT
  ③ Multi-master I2C-bus Tx/Rx data shift register—I2CDS
  ④ Multi-master I2C-bus address register—I2CADD

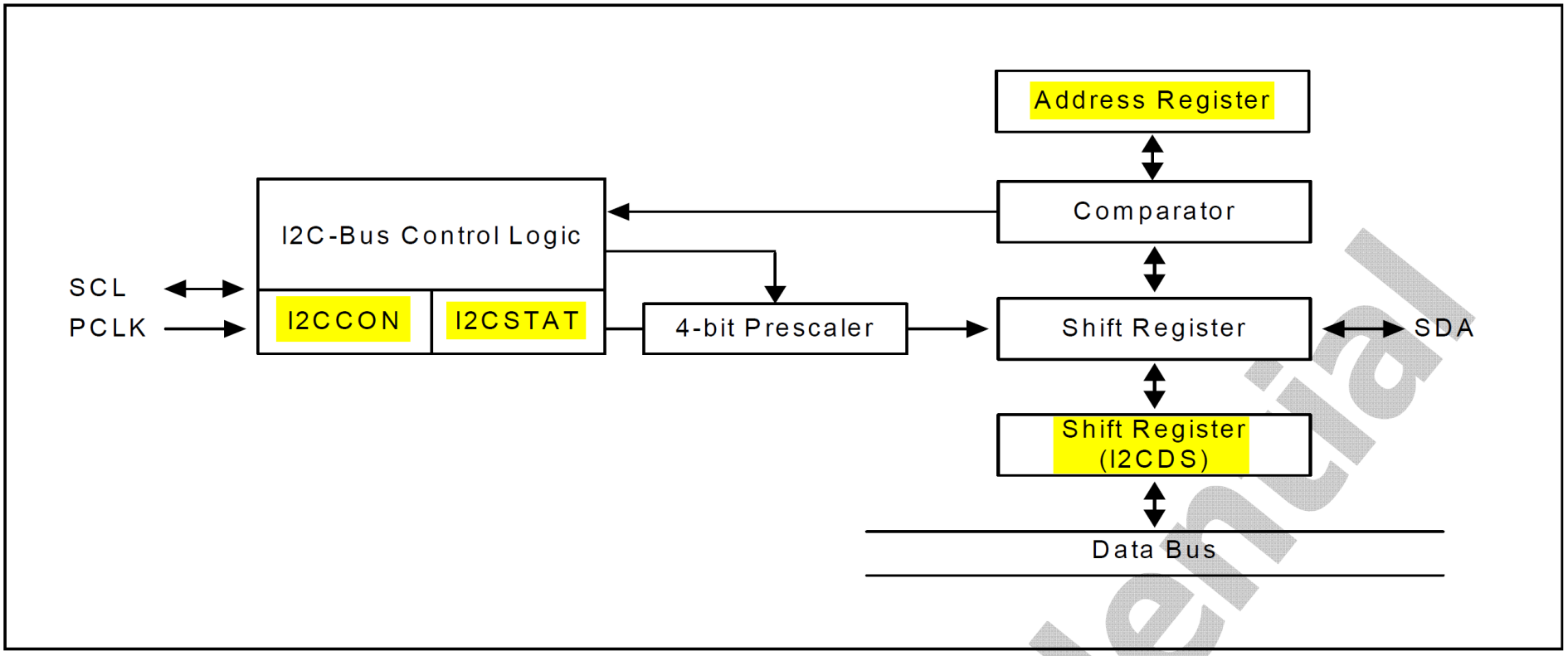


Figure 2-1 I^2C-Bus Block Diagram

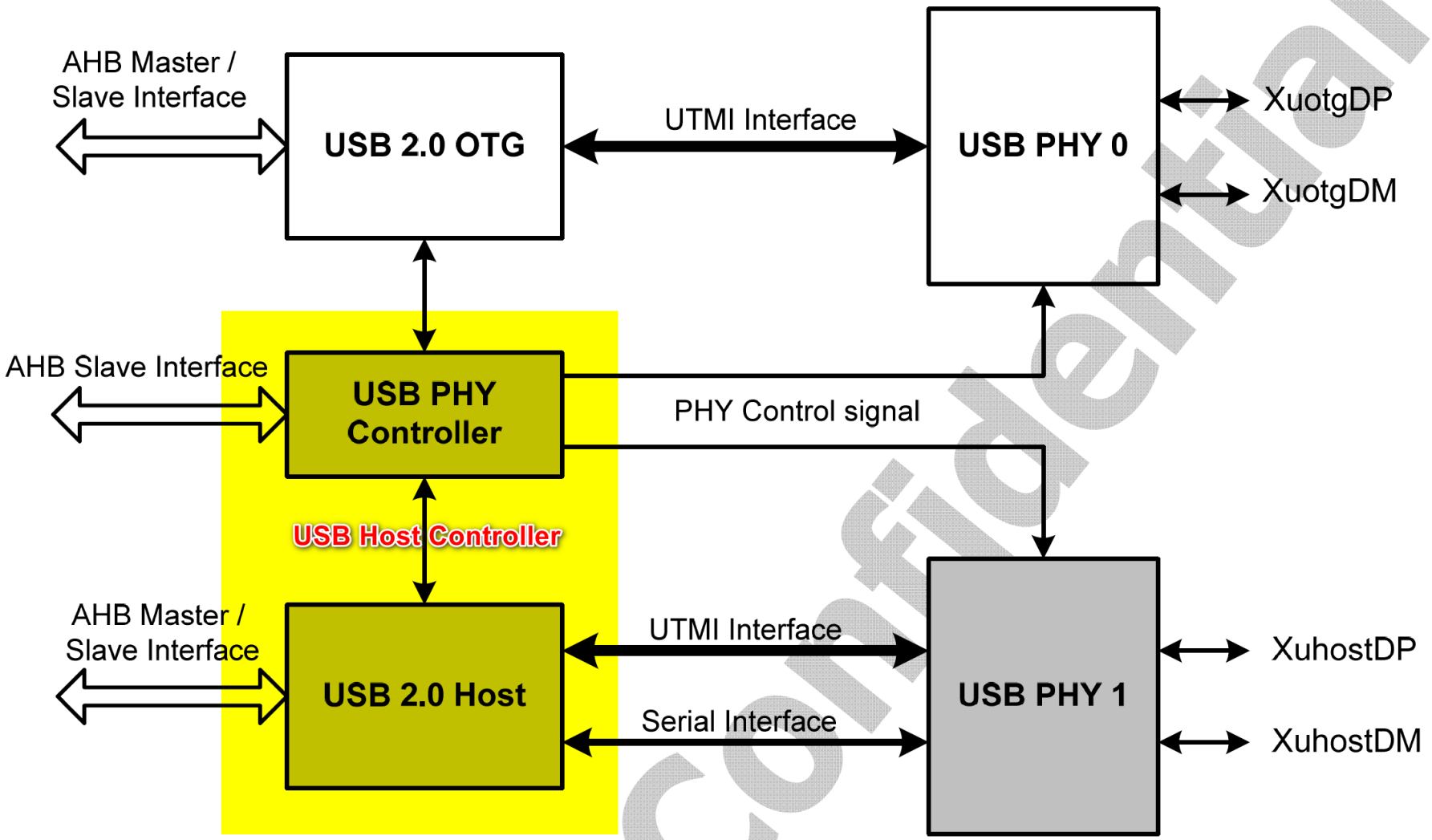
- **4通道，多主从控制IIC总线接口**
- **7-bit 地址模式**
- **串行，8-bit 优先，双向数据传输**
- **标准模式下，支持最大100kbps**
- **快速模式下，支持最大400kbps**
- **支持主、从收发，支持中断事件**

5.7 串行通信单元：SPI

- S5PV210提供串行外设接口（SPI）
- 基于SPI协议，可以同时发送和接收数据
- SPI下载

5.7 串行通信单元：USB

- S5PV210 支持单端口 USB host 接口
- 主要特性：
  - 兼容 EHCI Rev 1.0a 和 OHCI Rev1.0 规范
  - 遵循 USB Rev 2.0 规范
  - 遵循 USB Rev 1.1 规范
  - 支持高速外设（480 Mbps）
  - 支持电源管理特性，如
    完全挂起/恢复功能，包括远程唤醒
    过电流保护等



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Figure 4-1 USB System Block Diagram

5.7 串行通信单元：USB

- S5PV210 支持具有双重角色功能的 USB OTG (On-The-Go)
- 高速OTG还可配置为 Host-only 模式或者 Device-only 模式
- 主要特性：
  - 遵循补充 On-The-Go 的 USB 2.0 规范（Revision 1.0a）
  - 高速（480Mbps）全速（12Mbps）低速（1.5Mbps, Host only）
  - 支持 UTMI+ Level 3 接口
  - ……

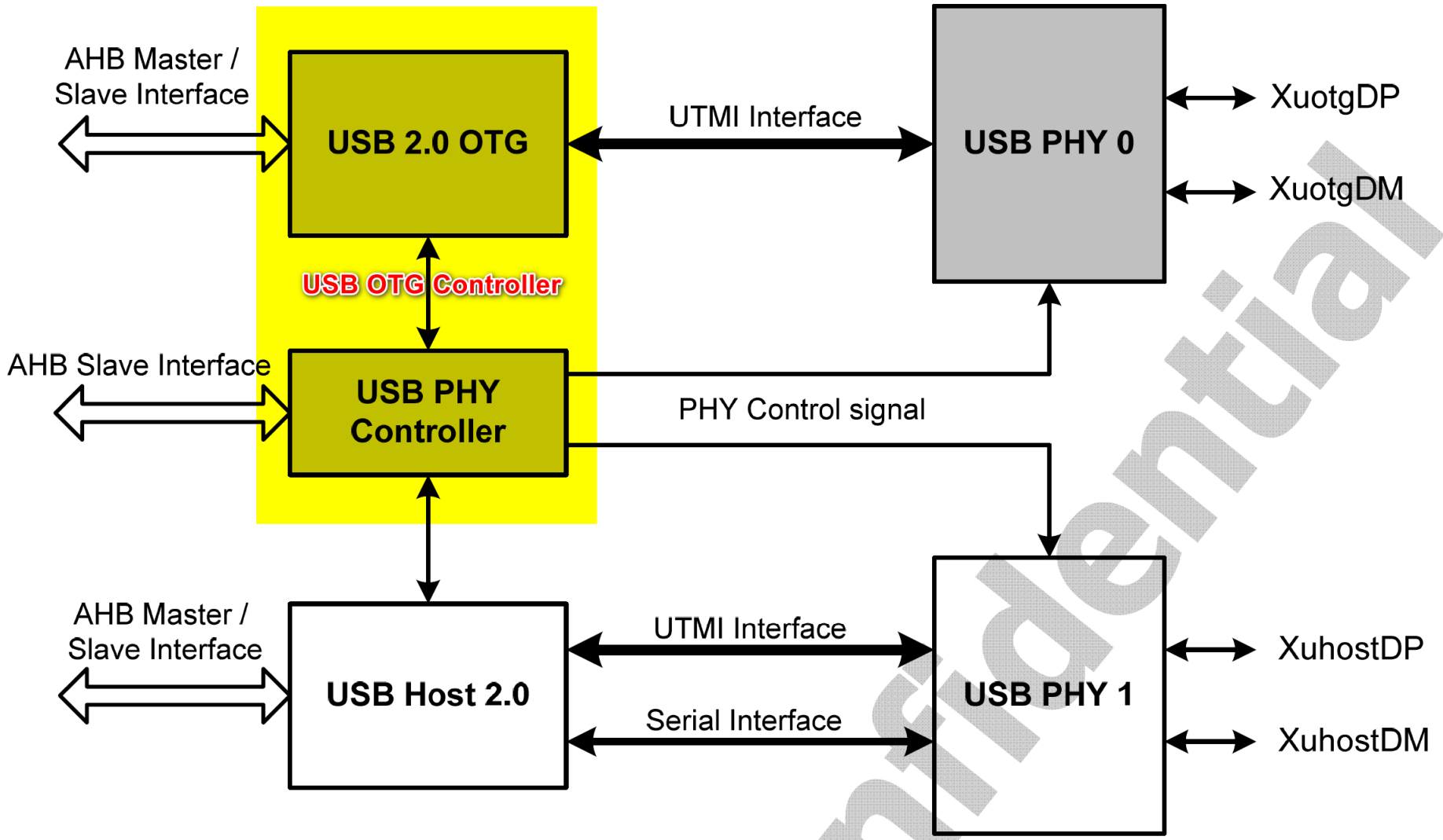


Figure 5-1 System Level Block Diagram

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5.8 通用I/O——GPIO

- S5PV210 提供：
  - 237 个多功能 GPIO 端口引脚
  - 142 个 Memory 端口引脚
- GPIO 的关键特性：
  - 控制 146 个GPIO中断
  - 控制 32 个外部中断
  - 有 237 个 GPIO 端口
  - Sleep 模式下控制引脚状态，GPH0, GPH1, GPH2, GPH3 除外

5.8 通用I/O——GPIO

根据 I/O 类型分类

2.1.3 S5PV210 INPUT/ OUTPUT TYPES

I/O Types	I/O Group	Description
A	GPA0, GPA1, GPC0, GPC1, GPD0, GPD1, GPE0, GPE1, GPF0, GPF1, GPF2, GPF3, GPH0, GPH1, GPH2, GPH3, GPI, GPJ0, GPJ1, GPJ2, GPJ3, GPJ4	Normal I/O (3.3V I/O)
B	GPB, GPG0, GPG1, GPG2, GPG3, MP0 GPIO	Fast I/O (3.3V I/O)
C	MP1, MP2 Momory IO	DRAM I/O (1.8V IO)

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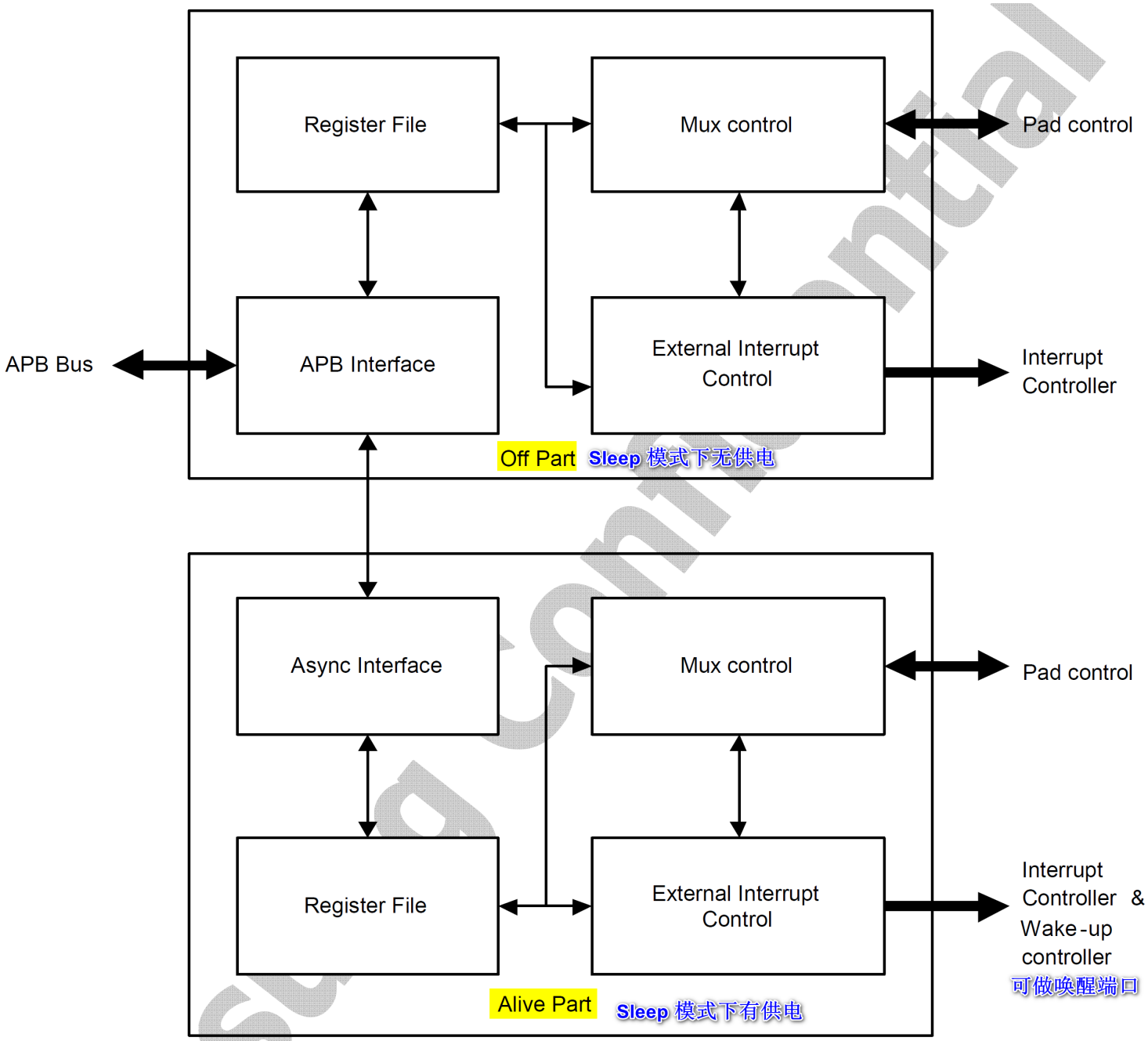


Figure 2-1 GPIO Block Diagram

2.1.5.3 Pin Mux Description 引脚复用

Pin Name	GPIO	Func0	Func1	Func2	Func3	Default	@Reset		Sleep	Pad Type
							PUD	I/O	State	
XuRXD[0]	GPA0[0]	UART_0_RXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuTXD[0]	GPA0[1]	UART_0_TXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuCTSn[0]	GPA0[2]	UART_0_CTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRTSn[0]	GPA0[3]	UART_0_RTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRXD[1]	GPA0[4]	UART_1_RXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuTXD[1]	GPA0[5]	UART_1_TXD				GPI	PD	I(L)	A1	PBIDIRSE_G
XuCTSn[1]	GPA0[6]	UART_1_CTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRTSn[1]	GPA0[7]	UART_1_RTSn				GPI	PD	I(L)	A1	PBIDIRSE_G
XuRXD[2]	GPA1[0]	UART_2_RXD		UART_AUDIO_RXD		GPI	PD	I(L)	A2	PBIDIRSE_G
XuTXD[2]	GPA1[1]	UART_2_TXD		UART_AUDIO_TXD		GPI	PD	I(L)	A2	PBIDIRSE_G
XuRXD[3]	GPA1[2]	UART_3_RXD	UART_2_CTSn			GPI	PD	I(L)	A2	PBIDIRSE_G
XuTXD[3]	GPA1[3]	UART_3_TXD	UART_2_RTSn			GPI	PD	I(L)	A2	PBIDIRSE_G
XspiCLK[0]	GPB[0]	SPI_0_CLK				GPI	PD	I(L)	A1	PBIDIRF_G

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2.2.1 REGISTER MAP

寄存器映射，寄存器描述，参考Datasheet P.115

Each Port Group has 2 types of control registers.

One works in normal mode, and the other works in power down mode (STOP, DEEP-STOP, SLEEP mode)

Normal registers (For example, GPA0CON, GPA0DAT, GPA0PUD, and GPA0DRV) are the former, and power down registers (For example, GPA0CONPDN, and GPA0PUDPDN) are the latter.

If, S5PV210 enter the power down mode, all configurations and Pull-down controls are selected by power down registers

掉电模式寄存器名带PDN后缀

Register	Address	R/W	Description	Reset Value
GPA0CON	0xE020_0000	R/W	Port Group GPA0 Configuration Register	0x00000000
GPA0DAT	0xE020_0004	R/W	Port Group GPA0 Data Register	0x00
GPA0PUD	0xE020_0008	R/W	Port Group GPA0 Pull-up/down Register	0x5555
GPA0DRV	0xE020_000C	R/W	Port Group GPA0 Drive Strength Control Register	0x0000
GPA0CONPDN	0xE020_0010	R/W	Port Group GPA0 Power Down Mode Configuration Register	0x00
GPA0PUDPDN	0xE020_0014	R/W	Port Group GPA0 Power Down Mode Pull-up/down Register	0x00
GPA1CON	0xE020_0020	R/W	Port Group GPA1 Configuration Register	0x00000000

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回顾：C语言

- 数据类型、运算符、程序控制、函数、数组、指针、*结构体
- 位运算
- 预处理
- 地址转换
- volatile限制符

位运算

- 与 &
  - (1) 提取某数的指定位：用 1
  - (2) 特定位清零：用 0
- 或 |
  - (1) 提取某数的指定位：用 0
  - (2) 置位某数的指定位：用 1
- 异或 ^
  - 取反某数的指定位：用 1
- 取反 ~
  - 取反某数的全部位
    - 与&结合，清零某数的指定位，对应汇编中的BIC
- 左移 <<
  - 相当于乘以2的幂次（幂次=移位数）
    - (1) 常用于某寄存器的特定位值 1，如：x = (0x1<<3) = 2_0100
    - (2) 也可代替乘法操作
- 右移 >>
  - 相当于除以2的幂次（幂次=移位数）
    - 可代替除法操作，无符号数与有符号数逻辑右移的结果有区别（用0还是1补全的问题）

预处理

- 宏定义：#define ... #undef
  - (1) 不带参数的宏，定义常量
  - (2) 带参数的宏，#define MAX(x,y) (x)>(y) ? (x):(y)
    注意与函数的区别
- 文件包含：#include
  - (1) #include<> — 直接按标准目录搜索
  - (2) #include" " — 先搜索当前目录，再搜索标准目录
- 条件编译

地址转换

```
#define rPCONA ( *(volatile unsigned *) 0x1D20000 )
```

volatile限制符

抑制编译器优化
提供特殊地址的稳定访问

场合
- (1) 存储器映射的硬件寄存器
- (2) 中断服务程序中修改的供其他程序检测的变量
- (3) 多任务环境下各任务间共享的标志

回顾：关于main函数的参数

```
int main(int argc, char *argv[])
{
        int i;
        printf("命令行参数的个数为：%d\n", argc);
        printf("当前程序名为：%s\n", arg[0]);
        if (argc > 1)
        {
                printf("其他参数为：\n");
                for(i=1; i<arg; i++)
                {
                        printf("%s\n", arg[i]);
                }
        }
        return 0;
}
```

- 两个内设形参用于接收命令行参数，argc中存放参数的个数，每个字符串指针指向一个命令行参数（第1个为当前程序名）